## 3.12.11

1. Mony's advice: capturing the whole video frame inside the FPGA

Calculation: 640\*480\*8=2457600 bits = 600 M4K blocks

This advice is not practical, because our FPGA has 105 M4K blocks.

1. Attached a file with the top description of the Symbol Generator block.

## Dictionary:

* command =
* type – add or remove (1 bit)
* x coordinate (4 bits)
* y coordinate (5 bits)
* address of the symbol in SDRAM (19 bits because: SDRAM depth is 2^20, therefore 20 bits for address. The symbol is saved in 2 rows in the SDRAM therefore the LSB is known – even or odd row)
* last command for this display (1 bit)

**TOTAL = 30 bits for the command**

* Symbol-block = the video frame is composed of 15x20 symbol blocks

## Description of the sub-blocks in the Symbol Generator

**Opcode\_unite block**

This block receives the data packages from the WBS.

Each command is divided between couple of WB packages. This block waits the needed time to unite this couple of packages to one command.

A valid signal will be generated when the command is united and ready to be sent.

This block will be implemented with a state machine. Each state in the FSM is for a new data package on the WB bus.

The FSM:

**Opcode\_FIFO block**

This FIFO receives the united command from the **Opcode\_unite block** and stores each command in a new entry.

Comment: this FIFO is optional. The other option is to send the united command to the **Opcode\_decoder block** directly. This FIFO's purpose is to prevent overflow with the command (in case receiving the commands is faster than processing them…)

**Opcode\_decoder block**

This block receives the united command and separates the fields:

1. Type – add or remove
2. X – the x coordinate of the symbol block
3. Y – the y of the symbol block
4. Address – the address of the symbol in the SDRAM

After separating the fields above, the **Opcode\_decoder block** turns to the RAM with the appropriate address and data:

1. Data\_RAM is the address of the symbol in the SDRAM
2. Adr\_RAM - The address in the RAM is: ROW = 20\*X + Y , because each RAM row corresponds to a symbol-block on the video frame
3. W\_en – enable signal to write to the RAM

In the command, we use the LSB to identify the last command for this display. In case it is the last command, then we finished updating the addresses in the RAM, and we are ready to read the symbols from the SDRAM.

**RAM block**

In the RAM, each row corresponds to the appropriate symbol-block

Size: 20x15 rows in the RAM

**RAM\_manager block**

When the display is ready and the RAM is updated, this block manages the read from the SDRAM through the WBM (address in the SDRAM, RAS, CAS etc.)

**FIFO\_CONTROL**

**FIFO\_A**

**FIFO\_B**